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Intel Optimization Reference Manual
The Intel® 64 and IA-32 architectures optimization reference manual provides information on current Intel microarchitectures. It describes code optimization techniques to enable you to tune your application for highly optimized results when run on current Intel® processors.

Intel® 64 and IA-32 Architectures Optimization Reference ...

Optimization Reference Manual Order Number: 248966-033 June 2016. Title: Intel® 64 and IA-32 Architectures Optimization Reference Manual Author: Intel Corporation Keywords: 64 architecture, IA-32, core processors, 248966 Created Date:

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version 043. Additional related specifications, application notes, and white papers are also available for download.

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Analyzing and Resolving multi-core non-scaling on Intel® Core™ 2 Processors For microarchitectural details, including events, programming the event counters, and the Software Optimization Reference Manual, please see the Intel® 64 and IA-32 Architectures Software Developer Manuals.

Tuning Guides and Performance Analysis Papers - Intel

In appendix C of the Intel 64 and IA-32 Architectures Optimization Reference Manual (available here), the latencies and throughput of instructions are listed. The documentation of the Intel C++ Compiler contains documentation of the intrinsics. The AVX Programming Reference and examples for using AVX are available on the AVX community page.

Links to instruction documentation - Intel Community

Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 2 (2A, 2B, 2C & 2D):
Instruction Set Reference, A-Z NOTE: The Intel 64 and IA-32 Architectures Software Developer's Manual consists of three volumes:

Intel® 64 and IA-32 Architectures Software Developer's Manual

Reference Manual for Intel® Math Kernel Library (Intel ... Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel

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The microarchitecture of Intel, AMD and VIA CPUs: An optimization guide for assembly programmers and compiler makers This manual contains details about the internal working of various microprocessors from Intel, AMD and VIA.

Software optimization resources. C++ and assembly. Windows ...

Ivy Bridge is almost identical to Sandy Bridge, which has its own section in the Intel Optimization Reference Manual (Intel document 248966). In the January 2016 revision (248966-032) this is section 2.3, with a processor block diagram in Figure 2-5 and lots of related information in Tables 2-12 through 2-24.

Good block diagram of Ivy Bridge ... - community.intel.com

The Optimization Reference Manual shows the Line Fill Buffers as sitting between the L1 Data Cache and the L2 cache in Figures 2-1 (Haswell) and 2-4 (Sandy Bridge). The text of Section 2.2.5.2 (Sandy Bridge L1 Data Cache) says: The L1 DCache can maintain up to 64 load micro-ops from allocation until retirement.

Solved: WB vs WC memory type - Intel Community

According to Intel 64 and IA-32 Architectures Optimization Reference Manual from May 2020, Volume 1, Chapter 2.5 Intel Instruction Set Architecture And Features Removed, HLE has been removed from Intel products released in 2019 and later. RTM is not documented as removed.

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Transactional Synchronization Extensions - Wikipedia

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