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Modern signal processing systems require more and more processing capacity as times goes on. Previously, large increases in speed and power efficiency have come from process technology improvements. However, lately the gain from process improvements have been greatly reduced. Currently, the way forward for high-performance systems is to use specialized hardware and/or parallel designs. Application Specific Integrated Circuits (ASICs) have long been used to accelerate the processing of tasks that are too computationally heavy for more general processors. The problem with ASICs is that they are costly to develop and verify, and the product life time can be limited with newer standards. Since they are very specific the applicable domain is very narrow. More general processors are more flexible and can easily adapt to perform the functions of ASIC based designs. However, the generality comes with a performance cost that renders general designs unusable for some tasks. The question then becomes, how general can a processor be while still being power efficient and fast enough for some particular domain? Application Specific Instruction set Processors (ASIPs) are processors that target a specific application domain, and can offer enough performance with power efficiency and silicon cost that is comparable to ASICs. The flexibility allows for the same hardware design to be used over several system designs, and also for multiple functions in the same system, if some functions are not used simultaneously. One problem with ASIPs is that they are more difficult to program than a general purpose processor, given that we want efficient software. Utilizing all of the features that give an ASIP its performance advantage can be difficult at times, and new tools and methods for programming them are needed. This thesis will present ePUMA (embedded Parallel DSP platform with Unique Memory Access), an ASIP architecture that targets algorithms with predictable data access. These kinds of algorithms are very common in e.g. baseband processing or multimedia applications. The primary focus will be on the specific features of ePUMA that are utilized to achieve high performance, and how it is possible to automatically utilize them using tools. The most significant features include data permutation for conflict-free data access, and utilization of address generation features for overhead free code execution. This sometimes requires specific information; for example the exact sequences of addresses in memory that are accessed, or that some operations may be performed in parallel. This is not always available when writing code using the traditional way with traditional languages, e.g. C, as extracting this information is still a very active research topic. In the near future at least, the way that software is written needs to change to exploit all hardware features, but in many cases in a positive way. Often the problem with current methods is that code is overly specific, and that a more general abstractions are actually easier to generate code from.

The International Workshop on Power and Timing Modeling, Optimization, and Simulation PATMOS 2002, was the 12th in a series of international workshops I previously held in several places in Europe. PATMOS has over the years evolved into a well-established and outstanding series of open European events on power and timing aspects of integrated circuit design. The increased interest, espe- ally in low-power design, has added further momentum to the interest in this workshop. Despite its growth, the workshop can still be considered as a very - cused conference, featuring high-level scienti?c presentations together with open discussions in a free and easy environment. This year, the workshop has been opened to both regular papers and poster presentations. The increasing number of worldwide high-quality submissions is a measure of the global interest of the international scienti?c community in the topics covered by PATMOS. The objective of this workshop is to provide a forum to discuss and inves- gate the emerging problems in the design methodologies and CAD-tools for the new generation of IC technologies. A major emphasis of the technical program is on speed and low-power aspects with particular regard to modeling, char- terization, design, and architectures. The technical program of PATMOS 2002 included nine sessions dedicated to most important and current topics on power and timing modeling, optimization, and simulation. The three invited talks try to give a global overview of the issues in low-power and/or high-performance circuit design.

World first Microprocessor INTEL 4004(a 4-bit Microprocessor)came in 1971 forming the series of first generation microprocessor.Science then with more and advancement in technology ,there have been five Generations of Microprocessors.However the 8085,an 8-bit Microprocessor,is still the most popular Microprocessor.The present book provided a simple explanation,about the Microprocessor,its programming and interfacing.The book contains the description,mainly of the 8-bit programmable Interrupt Interval Timer/Counter 8253,Programmable communication Interface 8251,USART 8251A and INTEL 8212/8155/8256/8755 and 8279.

This book is a comprehensive, step-by-step guide to software engineering.This book provides an introduction to software engineering for students in undergraduate and post graduate programs in computers.

Although adaptive filtering and adaptive array processing began with research and development efforts in the late 1950's and early 1960's, it was not until the publication of the pioneering books by Honig and Messerschmitt in 1984 and Widrow and Stearns in 1985 that the field of adaptive signal processing began to emerge as a distinct discipline in its own right. Since 1984 many new books have been published on adaptive signal processing, which serve to define what we will refer to throughout this book as conventional adaptive signal processing. These books deal primarily with basic architectures and algorithms for adaptive filtering and adaptive array processing, with many of them emphasizing practical applications. Most of the existing textbooks on adaptive signal processing focus on finite impulse response (FIR) filter structures that are trained with strategies based on steepest descent optimization, or more precisely, the least mean square (LMS) approximation to steepest descent. While literally hundreds of archival research papers have been published that deal with more advanced adaptive filtering concepts, none of the current books attempt to treat these advanced concepts in a unified framework. The goal of this new book is to present a number of important, but not so well known, topics that currently exist scattered in the research literature. The book also documents some new results that have been conceived and developed through research conducted at the University of Illinois during the past five years.

This book constitutes the refereed proceedings of the 10th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2000, held in GÄttingen, Germany in September 2000. The 33 revised full papers presented were carefully reviewed and selected for inclusion in the book. The papers are organized in sections on RTL power modeling, power estimation and optimization, system-level design, transistor level design, asynchronous circuit design, power efficient technologies, design of multimedia processing applications, adiabatic design and arithmetic modules, and analog-digital circuit modeling.

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